CLAIMS

1. A reactance adjuster for adjusting reactance caused by a communication apparatus that transmits and/or receives a signal via an electric field transmittable medium (121) and said electric field transmittable medium (121),

a signal generation section (5, 6) generating a probe signal,

an electrode (123) inducing an electric field based on said probe signal in said electric field transmittable medium (121),

a resonance section (7) that is connected between said signal generation section (5, 6) and said electrode (123) and induces a series resonance by adjusting reactance against parasitic capacitance induced between said electric field transmittable medium (123), said communication apparatus, and an earth ground,

an adjusting signal generation section (13) outputting alternatingly a high level signal and a low level signal to said resonator section (7),

an electric field detection section (15) that receives an electric field in said electric field transmittable medium (121) and generates an electric signal based on the received electric field,

a signal output section including a first electric charge storing means (C1) storing an electric charge in accordance

with said electric signal while said adjusting signal generation section (13) outputs a high level signal to said resonator section (7), a second electric charge storing means (C2) storing an electric charge in accordance with said electric signal while said adjusting signal generation section (13) outputs a low level signal to said resonator section (7), and a voltage comparator (10) comparing a voltage across said first electric charge storing means (C1) and a voltage across said second electric charge storing means (C2) to output a predetermined signal in accordance with the comparison result, and

a control section (19; 20; 21; 23; 230) that outputs a voltage having a constant voltage value to said resonator section (7) while either one of said first and said second electric charge storing means (C1, C2) is storing an electric charge, and inputs said predetermined signal to output a voltage based on the inputted predetermined signal to said resonator section (7) while said first and second electric charge storing means stop storing an electric charge.

2. A reactance adjuster as recited in claim 1, wherein said control section (19) comprises:

a constant voltage source (12) outputting the voltage having a predetermined voltage value,

an integrator (11; 100; 200; 203) outputting a voltage having said constant voltage value when receiving the voltage

having said predetermined voltage value and outputting a voltage based on said predetermined signal when receiving said predetermined voltage to said resonator section (7),

an output switching section (4) inputting selectively the voltage having said predetermined voltage value or said predetermined signal, thus outputting said voltage having said predetermined voltage value to said integrator (11) while either one of said first and said second electric charge storing means (C1, C2) is storing an electric charge and outputting said predetermined signal to said integrator (11) when said first and second electric charge storing means stop storing an electric charge.

3. A reactance adjuster as recited in claim 2, wherein said integrator (100) comprises:

a first connection means (SW1), one end of which is connected to a positive electrode of a voltage source (Vdd) outputting a predetermined voltage,

a second connection means (SW2), one end of which is connected to the other end of said first connection means (SW1) and the other end of which is connected to a negative electrode of said voltage source,

a first comparison means (211; 221; 231) comparing a predetermined first threshold voltage (V1) and said predetermined signal to output a signal for turning on said first connection means (SW1) when said predetermined signal

is lower than said first threshold voltage (V1),

a second comparison means (212; 222; 232) comparing a second threshold voltage (V2) higher than said first threshold voltage (V1) and said predetermined signal to output a signal for turning on said connection means (SW2) when said predetermined signal is higher than said second threshold voltage (V2), and

a capacitor (213; 227; 237), one end of which is connected to said other end of said first connection means and the other end of which is connected to said negative electrode.

4. A reactance adjuster as recited in claim 3, wherein said integrator (200) further comprises:

a first current source (225) provided between said positive electrode and said first connection means (SW1),

a third comparison means (223) that compares said predetermined signal and a third threshold voltage (V3) lower than said first threshold voltage (V1) and outputs a current control signal to said first current source (225) so that a first constant current having a predetermined current value flows from said first current source (225) when said predetermined signal is lower than said threshold voltage (V3) or a second constant current smaller than said first constant current flows from said first current source (225) when said predetermined signal is higher than said third threshold voltage (V3) and lower than said first threshold

voltage (V1),

a second current source (236) provided between said negative electrode and said second connection means, and

a fourth comparison means (224) that compares said predetermined signal and said fourth threshold voltage (V4) higher than said second threshold voltage (V2) and outputs a current control signal to said second current source (236) so that a third constant current flows from said second current source (236) when said predetermined signal is higher than said fourth threshold voltage or a fourth current smaller than said third current flows from said second current source (236) when said predetermined signal is higher than said second threshold voltage (V2) and lower than said fourth threshold voltage (V4).

5. A reactance adjuster as recited in claim 3, wherein said integrator (203) further comprises:

a first variable current source (235) provided between said positive electrode and said first connection means (SW1),

a first differential amplifying means (233) that compares said predetermined signal and said first threshold voltage (V1) and outputs a current control signal to said first variable current source (235) so that the smaller said determined signal is, the larger the current flows from said variable current source (235),

a second variable current source (236) provided between said negative electrode and said second connection means (SW2), and

a second differential amplifying means (234) that compares said predetermined signal and said second threshold voltage (V2) and outputs a current control signal to said second variable current source (236) so that the higher said predetermined signal is, the larger the current flows from said second variable current source (236).

6. A reactance adjuster as recited in claim 3, wherein said integrator further comprises:

a first variable resistor provided between said positive electrode and said first connection means (SW1),

a first differential amplifying means that compares said predetermined signal and said first threshold voltage and outputs a resistance value control signal to said first variable resistor so that the lower said predetermined signal is, the lower the resistance of said first variable resistor becomes,

a second variable resistor provided between said negative electrode and said second connection means, and

a second differential amplifying means that compares said predetermined signal and said second threshold voltage and outputs a resistance value control signal to said second variable resistor so that the higher said predetermined

signal is, the lower the resistance of said second variable resistor becomes.

7. A reactance adjuster as recited in claim 1, wherein said control section (20) comprises:

a first p-channel Metal Oxide Semiconductor Field Effect Transistor (MOS-FET) (pMOS1) that turns off while either one of said first and said second electric charge storing means (C1, C2) is storing an electric charge and turns on when said first and said second electric charge storing means (C1, C2) stop storing,

a second p-channel MOS-FET (pMOS2) connected in series with said first p-channel MOS-FET (pMOS1), said second p-channel MOS-FET (pMOS2) turning on when said voltage comparator (10) determines that a voltage across said first electric charge storing means (C1) is higher than a voltage across said second electric charge storing means (C2) and turning off when said voltage comparator (10) determines that a voltage across said first electric charge storing means (C1) is lower than a voltage across said second electric charge storing means (C2),

a first n-channel MOS-FET (nMOS1) connected in series with said second p-channel MOS-FET (pMOS2), said first n-channel MOS-FET (nMOS1) turning on when said voltage comparator (10) determines that a voltage across said first electric charge storing means (C1) is lower than a voltage

across said second electric charge storing means (C2) and turning off when said voltage comparator (10) determines that a voltage across said first electric charge storing means (C1) is higher than a voltage across said second electric charge storing means (C2),

a second n-channel MOS-FET (nMOS2) connected in series with said first n-channel MOS-FET (nMOS1), said second n-channel MOS-FET (nMOS2) turning off when either one of said first and said second electric charge storing means (C1, C2) is storing an electric charge and turning on when said first and said second electric charge storing means (C1, C2) stop storing, and

a capacitor (Cp), one end of which is connected to a node between said second p-channel MOS-FET (pMOS2) and said first n-channel MOS-FET (nMOS1) and the other end of which is connected to the earth ground.

8. A reactance adjuster as recited in claim 7, wherein said control section (21) further comprises:

a first reference voltage source (SX) outputs a predetermined first reference voltage,

a first voltage comparator (X) comparing said predetermined signal and said first reference voltage to output a voltage in accordance with the comparison result to said second p-channel MOS-FET (pMOS2),

a second reference voltage source outputting a

predetermined second reference voltage, and

a second voltage comparator (Y) comparing said predetermined signal and said second reference voltage to output a voltage in accordance with the comparison result to said first n-channel MOS-FET (nMOS1).

9. A reactance adjuster as recited in claim 8, wherein said control section (23) further comprises:

a first variable resistor (RX) connected between said first p-channel MOS-FET (pMOS1) and said second p-channel MOS-FET (pMOS2),

a third comparator comparing said first reference voltage and said predetermined signal to output a signal in accordance with the comparison result so as to control resistance of said first variable resistor (RX),

a second variable resistor (RY) connected between said first n-channel MOS-FET (nMOS1) and said second n-channel MOS-FET (nMOS2), and

a fourth comparator (AY) comparing said second reference voltage and said predetermined signal to output a signal in accordance with the comparison result so as to control resistance of said second variable resistor (RY).

10. A reactance adjuster as recited in claim 8, wherein said control section (230) further comprises:

a first current source (250) connected between said first

p-channel MOS-FET (pMOS1) and said second p-channel MOS-FET (pMOS2),

a third signal comparison means (223) that compares said predetermined signal and a third reference voltage lower than said first reference voltage and outputs a current control signal to said first current source (250) so that said first current source (250) flows a first constant current when said predetermined signal is lower than said third reference voltage or said first current source (250) flows a second constant current smaller than said first constant current when said predetermined signal is higher than said third reference voltage and lower than said first reference voltage,

a second current source (226) connected between said first n-channel MOS-FET (nMOS1) and said second n-channel MOS-FET (nMOS2), and

a fourth signal comparator (224) that compares said predetermined signal and a fourth reference voltage higher than said second reference voltage and outputs a current control signal to said second current source (226) so that said second current source (226) flows a third constant current when said predetermined signal is higher than said fourth reference voltage or said second current source (226) flows a fourth constant current smaller than said third constant current when said predetermined signal is higher than said second reference voltage and lower than said fourth

reference voltage.

11. A reactance adjuster as recited in either claim 4 or 10, wherein said first constant current and said third constant current have a same current value, and wherein said second constant current and said fourth constant current have a same current value.

12. A reactance adjuster as recited in claim 8, wherein said control section (21) further comprises:

a first variable current source connected between said first p-channel MOS-FET (pMOS1) and said second p-channel MOS-FET (pMOS2),

a first differential amplifying means comparing said predetermined signal and said first reference voltage to output a current control signal to said first variable current source so that the smaller said predetermined signal is, the larger the current flows from said first variable current source,

a second variable current source connected between said first n-channel MOS-FET (nMOS1) and said second n-channel MOS-FET (nMOS2), and

a second differential amplifying means comparing said predetermined signal and said second reference voltage to output a current control signal to said second variable current source so that the larger said predetermined signal

is, the larger the current flows from said second variable current source.

13. A reactance adjuster as recited in claim 1, wherein said signal output section further comprises a detection means (8) detecting an amplitude of said electric signal to output a detection voltage in accordance with said amplitude, and a filter (9) eliminating a high harmonics component from said detection voltage.

14. A reactance adjuster as recited in claim 1, wherein said signal output section further comprises a sampling means (25) sampling said electric signal to output a voltage in accordance with said electric signal.

15. A reactance adjuster as recited in claim 1, wherein said signal output section further comprises a peak-hold means (25) holding a peak value of an amplitude of said electric signal to output a voltage in accordance with the peak value.

16. A reactance adjuster as recited in claim 15, wherein said peak-hold means (26) comprises an addition means (26) detecting said peak value at a predetermined number of times to add said peak value.

17. A reactance adjuster as recited as any one of claims

1 to 16, wherein said control section (19; 20; 21; 23; 230) further comprises an adder (14) adding a voltage based on a voltage having said constant voltage value outputted to said resonance section (7) from said control section (19; 20; 21; 23; 230) or a voltage based on said predetermined signal and a high level signal or a low level signal being alternatingly outputted to said resonance section (7) from said adjusting signal generation section (13).

18. A signal processing circuit comprising:

a first connection means (SW1), one end of which is connected to a positive electrode of a voltage source (Vdd) outputting a predetermined voltage,

a second connection means (SW2), one end of which is connected to the other end of said first connection means (SW1) and the other end of which is connected to a negative electrode of said voltage source,

a first comparison means (211) that compares a predetermined first threshold voltage (V1) and an input voltage and outputs a signal to turn on said first connection means (SW1) when said input voltage is lower than said first threshold voltage (V1),

a second comparison means (212) that compares an input voltage and a second threshold voltage (V2) higher than said first threshold voltage (V1) and outputs a signal to turn on said second connection means (SW2) when said input voltage

is higher than said second threshold voltage (V2), and

a capacitor (213), one end of which is connected to said other end of said connection means (SW1) and the other end of which is connected to said negative electrodes.

19. A signal processing circuit as recited in claim 18, further comprising:

a first current source (225) provided between said positive electrode and said first connection means (SW1),

a third comparison means (223) that compares an input voltage and a third threshold voltage (V3) lower than said first threshold voltage (V1) and output a current control signal to said first current source (225) so that a first constant current flows from said first current source (225) when said input voltage is lower than said third threshold voltage (V3) or a second constant current smaller than said first constant current flows from said first current source (225) when said input voltage is higher than said third threshold voltage (V3) and lower than said first threshold voltage,

a second current source (226) provided between said negative electrode and said second connection means (SW2), and

a fourth comparison means (224) that compares an input voltage and a fourth threshold voltage (V4) higher than said second threshold voltage (V2) and outputs a current control

signal to said second current source (226) so that a third constant current flows from said second current source (226) when said input voltage is higher than said fourth threshold voltage (V4) or a fourth constant current smaller than said third constant current flows from said second current source (226) when said input voltage is higher than said second threshold voltage (V2) and lower than said fourth threshold voltage (V4).

20. A signal processing circuit as recited in claim 18, further comprising:

a first variable current source (235) provided between said positive electrode and said first connection means (SW1),

a first differential amplifying means (233) that compares an input voltage and said first threshold voltage (V1) and outputs a current control signal to said first variable current source (235) so that the lower said input voltage is, the larger the current flows from said first variable current source (235),

a second variable current source (236) provided between said negative electrode and said second connection means (SW2), and

a second differential amplifying means (234) that compares an input voltage and said second threshold voltage (V2) and outputs a current control signal to said second

variable current source (236) so that the higher said input voltage is, the larger the current flows from said second variable current source (236).

21. A signal processing circuit as recited in claim 18, further comprising:

a first variable resistor provided between said positive electrode and said first connection means (SW1),

a first differential amplifying means that compares an input voltage and said first threshold voltage and outputs a resistance control signal to said first variable resistor so that the lower said input voltage is, the smaller the resistance of said first variable resistor becomes,

a second variable resistor provided between said negative electrode and said second connection means, and

a second differential amplifying means that compares an input voltage and said second threshold voltage and outputs a resistance control signal to said second variable resistor so that the higher said input voltage is, the lower the resistance of said second variable resistor becomes.

22. A transceiver transmitting and receiving data via an electric field transmittable medium, comprising:

a reactance adjuster as recited in any one of claims 1 to 17,

an interface portion (122) for use in communication with

a computer managing data to be transmitted,

a data signal generation portion provided between said interface portion (122) and said resonance portion, said data signal generation portion generating a signal wave including data to be transmitted obtained via said interface portion (122) to supply the data to said resonance portion (7), and

a receiving portion (32) provided between said interface portion (122) and said electrode (123), said receiving portion (32) detecting an electric field in said electric field transmittable medium via said electrode (123) and obtaining data to be received from the electric field detected so as to supply the data to said interface portion (122).

23. A transceiver as recited in claim 22, wherein said receiving portion (32) inputs a converted electric signal from said electric field detection portion (15) and obtains data to be received from the electric signal to supply to said interface portion (122).

24. A transceiver as recited in any one of claims 22 and 23, wherein said data signal generation portion generates said probe signal.

25. A transmitter transmitting data via an electric field transmittable medium (121), comprising:

a reactance adjuster as recited in any one of claims 1

to 17,

an interface portion (122) for use in communication with a computer managing data to be transmitted, and

a data signal generation portion provided said interface portion (122) and said resonance portion, said data signal generation portion generating a signal wave including data to be transmitted obtained via said interface portion (122) to supply to said resonance portion (7).

26. A transmitter as recited in claim 26, wherein said data signal generation portion generates said probing signal.

27. A method of adjusting reactance caused by a communication apparatus transmitting/receiving data via an electric field transmittable medium (121) and said electric field transmittable medium, said method comprising:

inducing an electric field based on a probe signal generated from a signal generation portion (5, 6) in said electric field transmittable medium (121) via an electrode (123),

outputting alternatingly a high level signal and a low level signal to a resonance portion (7) generating a series resonance by adjusting a reactance value against parasitic capacitance caused between said electric field transmittable medium (121), a communication apparatus, and an earth ground, said resonance portion (7) being connected in series between

said signal generation portion (5, 6) and said electrode (123),

receiving the electric field in said electric field transmittable medium (121) via said electrode (123),

generating an electric signal based on the received electric field,

storing an electric charge based on said electric signal in a first electric charge storing means (C1) when outputting a high level signal to said resonance portion (7), storing an electric charge based on said electric signal in a second electric charge storing means (C2) when outputting a low level signal to said resonance portion (7), and outputting a predetermined signal based on a voltage difference between a voltage across said first electric charge storing means (C1) and a voltage across said second electric charge storing means (C2), and

outputting a voltage having a constant voltage value to said resonance portion (7) when either one of said first electric charge storing means (C1) and said second electric charge storing means (C2) is storing electric charge and outputting a voltage based on said predetermined signal to said resonance portion (7) when said first electric charge storing means (C1) and said second electric charge storing means (C2) stop storing.

28. A method of transmitting signal via an electric field

transmittable medium (121), comprising:

inducing an electric field based on a probe signal generated from a signal generation portion (5, 6) in said electric field transmittable medium (121) via an electrode (123),

outputting alternatingly a high level signal and a low level signal to a resonance portion (7) generating a series resonance by adjusting a reactance value against parasitic capacitance caused between said electric field transmittable medium (121), a communication apparatus, and an earth ground, said resonance portion (7) being connected in series between said signal generation portion (5, 6) and said electrode (123),

receiving an electric field in said electric field transmittable medium (123) via said electrode (123),

generating an electric signal based on the received electric field,

storing an electric charge based on said electric signal in a first electric charge storing means (C1) when outputting a high level signal to said resonance portion (7), storing an electric charge based on said electric signal in a second electric charge storing means (C2) when outputting a low level signal to said resonance portion (7), and outputting a predetermined signal based on a voltage difference between a voltage across said first electric charge storing means (C1) and a voltage across said second electric charge storing means

(C2),

outputting a voltage having a constant voltage value to said resonance portion (7) when either one of said first and said second electric charge storing means (C1, C2) is storing electric charge and outputting a voltage based on said predetermined signal when said first and said second electric charge storing means (C1, C2) stop storing, and

supplying a signal wave including data to be transmitted to said electrode.

29. A method of receiving signal via an electric field transmittable medium (121), comprising:

inducing an electric field based on a probe signal generated from a signal generation portion (5, 6) in said electric field transmittable medium (121) via an electrode (123),

outputting alternatingly a high level signal and a low level signal to a resonance portion (7) generating a series resonance by adjusting a reactance value against parasitic capacitance caused between said electric field transmittable medium (121), a communication apparatus, and an earth ground, said resonance portion (7) being connected in series between said signal generation portion (5, 6) and said electrode (123),

receiving the electric field in said electric field transmittable medium (121) via said electrode (123),

generating an electric signal based on the received electric field,

storing an electric charge based on said electric signal in a first electric charge storing means (C1) when outputting a high level signal to said resonance portion (7), storing an electric charge based on said electric signal in a second electric charge storing means (C2) when outputting a low level signal to said resonance portion (7), and outputting a predetermined signal based on a voltage difference between a voltage across said first electric charge storing means (C1) and a voltage across said second electric charge storing means (C2),

outputting a voltage having a constant voltage value to said resonance portion (7) when either one of said first and said second electric charge storing means (C1, C2) is storing electric charge and outputting a voltage based on said predetermined signal when said first and said second electric charge storing means (C1, C2) stop storing,

receiving the electric field in said electric field transmittable medium via said electrode to generate a receiving data electric signal including data to be received, and

demodulating said receiving data electric signal to obtain said data.